CLAIMS

What is claimed is:

1.   A decoding unit for decoding a received signal comprising:

a plurality of soft-decoders, each soft-decoder sampling the received signal at a different time within a symbol period and outputting two values, the first value comprising a preliminary decoded value and the second value comprising an ambiguity indicator; and

a logic device coupled to the each of the soft-decoders, for determining a decoded value for each symbol based on one or more preliminary decoded values and ambiguity indicators.

2.   The decoding unit of Claim 1, wherein each of the soft-decoders are identical.

3.   The decoding unit of Claim 1, wherein each soft-decoder comprises:

a first comparator with inputs comprising the received signal and a first reference voltage;

a second comparator with inputs comprising the received signal and a second reference voltage; and

a third comparator with inputs comprising the received signal and a third reference voltage.

4.   The decoding unit of Claim 1, wherein each soft-decoder comprises a plurality of comparators and one or more logical AND gates.

5.   The decoding unit of Claim 1, further comprising a plurality of delay elements coupled to the soft-decoders.

6.   The decoding unit of Claim 1, further comprising a plurality of delay elements coupled to the soft-decoders, each delay element delaying the received signal by a different amount.

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7. The decoding unit of Claim 1, further comprising a plurality of delay elements coupled to the soft-decoders, each delay element delaying the clock signal by a different amount.

8. A decoding unit for decoding a received signal comprising:

an asynchronous soft-decoder that continuously samples the received signal;

a plurality of first delay elements coupled to a first soft-decoder, each first delay element generating a different delay relative to another first delay element and producing a first ambiguity indicator;

a plurality of second delay elements coupled to a second soft-decoder output, each second delay element generating a different delay relative to another second delay element and producing a preliminary decoded output; and

a logic device coupled to the each of the delay elements, for determining a decoded value based on one or more the preliminary decoded output and ambiguity indicators.

9. The decoding unit of Claim 8, wherein the soft-decoder comprises:

a first comparator with inputs comprising the received signal and a first reference voltage;

a second comparator with inputs comprising the received signal and a second reference voltage; and

a third comparator with inputs comprising the received signal and a third reference voltage.

10. The decoding unit of Claim 8, wherein the soft-decoder comprises a plurality of comparators and one or more logical AND gates.

11.   A decoding unit for decoding a received signal comprising:

an analog-to-digital converter for sampling the received signal faster than once every symbol period of the received signal;

a processor coupled to the converter for grouping a subset of sampled values derived from the single symbol period, for examining the subset of values and determining a value closest to an optimum sampling time based on a principle of generalized maximum likelihood, for decoding the value closest to the optimum sampling time and outputting that sample as the decoded symbol.

12.   The decoding unit of Claim 11, further comprising a clock recovery unit coupled to the converter for providing a clock signal.

13.   The decoding unit of Claim 11, wherein the processor calculates the value closest to the optimum sampling time by:

computing an absolute difference between each value and a nearest level corresponding to a decoded symbol

finding a value which has a smallest absolute difference from the subset of values; and

taking the sample with the smallest absolute difference as the sample closest to the optimum sampling time.

14.   A method for decoding a received signal comprising:

receiving a signal;

estimating an optimal timing offset on a symbol-by-symbol basis; and

decoding the communicated signal using generalized maximum likelihood estimation with the estimated optimal timing offset.

15.   The method of Claim 14, wherein estimating an optimal timing offset on a symbol-by-symbol basis further comprises generating an ambiguity indicator and a preliminary decoded value for a sample.

16.   The method of Claim 14, wherein estimating an optimal timing offset on a symbol-by-symbol basis further comprises:

dividing the received signal into a plurality of received signals;

delaying the one or more received signals by different amounts of time.

17.   The method of Claim 14, wherein estimating an optimal timing offset on a symbol-by-symbol basis further comprises:

dividing an ambiguity indicator signal and a preliminary decoded value signal derived from the received signal; and

delaying each ambiguity indicator signal and each preliminary decoded value signal by different amounts of time.

18.   The method of Claim 14, wherein estimating an optimal timing offset on a symbol-by-symbol basis further comprises:

determining a clock signal from the received signal;

taking multiple samples of the received signal in accordance with the clock signal; and

converting the received signal into the digital domain based on the multiple samples.

19.   The method of Claim 14, wherein decoding the received signal using generalized maximum likelihood estimation with an optimal sampling point further comprises determining a sample timing index from one or more ambiguity indicators.

5   20.   The method of Claim 14, wherein decoding the received signal using generalized maximum likelihood estimation with an optimal sampling point further comprises identifying a symbol that corresponds to a selected timing index.